CIS 4930 / CIS 6930 CMOS VLSI Design
Spring 2004
Instructor: Dr. Srinivas Katkoori

Handout on CADENCE Virtuoso Layout Editor

Setting up your user environment

(a) Create a new directory, say `cmos`.
sunray % `mkdir cmos`

(b) Set up the initialization environment for Virtuoso, by running a script called `digital-init`, in the newly created directory.
sunray % `cd cmos`
sunray % `digital-init`

(c) You will need three *technology files* to create your CMOS layouts. These files are:
(a) `project.tf`,
(b) `divaDRC.rul`, and
(c) `divaERC.rul`

Download these files from the class web page the first time you use Virtuoso. You can use the same technology files for all other designs. You will need to copy these three files to the current library file as explained below.

Creating a New Library

(a) Start Virtuoso by typing the command at the prompt
sunray % `digital-icfb &`
This pops up two separate windows on your screen (Figure 1), with the names "**Library Manager**" and "**icfb-Log**".

(b) On the *Library Manager* window, create a new library by selecting
File → New → Library
This pops up a window with the label "**New Library**". Type a library name in the *Name* field. As an example, let the library name be "**mylib**". Click "OK". This pops up a window querying about the *technology* file for this library. Select the button that says "**Compile a new techfile**". When you click "**OK**", a window pops up (Figure 2) asking for the technology file. Enter the file name as "project.tf".

(c) Go to a sunray terminal and copy the following technology files `divaDRC.rul` and `divaEXT.rul` to the current library directory "**mylib**".

Written by Praveen Samudrala, Fall 2001. Revised by Vyas Krishnan, Spring 2004

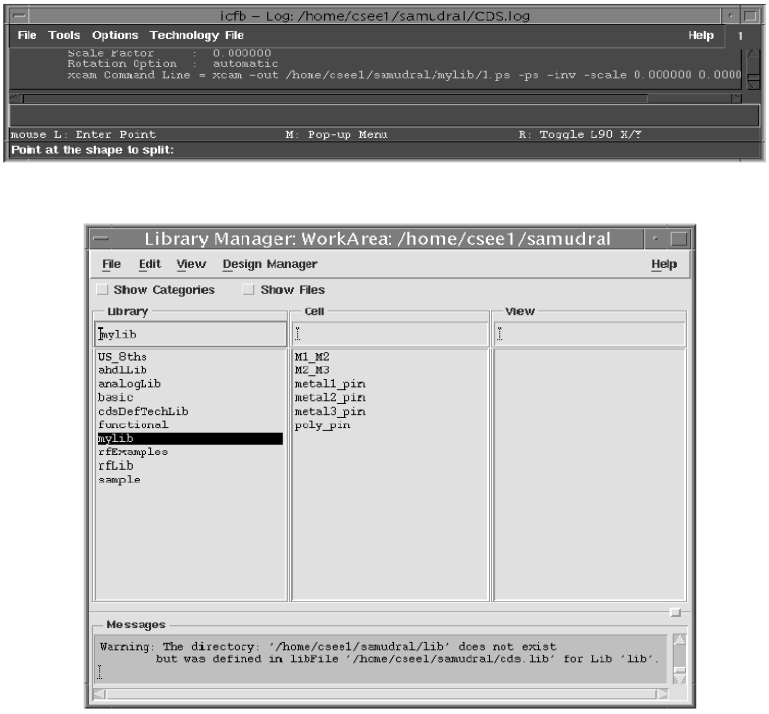

Figure.1

Figure.2

Creating a New Cell View

(d) Create a cell view by selecting **File→New→Cellview** from **Library Manager** window (Figure 3).

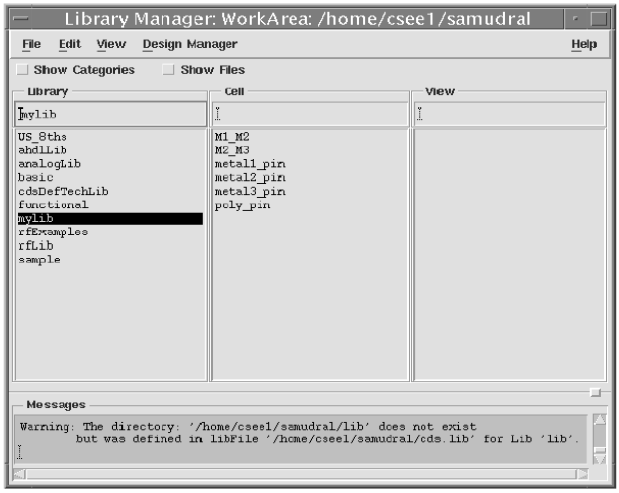

Figure. 3

Select the library name as "**mylib**"(the library name that you entered before) and type the cell name, say "**inverter**" and select the Tool as "**Virtuoso**" as in Fig.5.

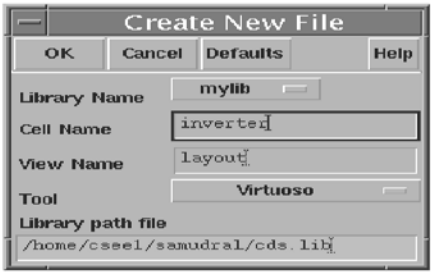

Figure. 4

On clicking "OK", two windows, namely the **LSW** (*Layer Select Window*) window (Figure. 5), and the **Layout Editor** window (Figure. 6) open up.

Figure. 5

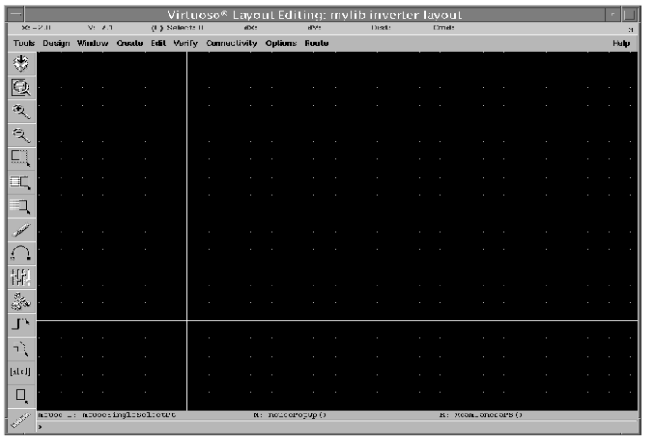

Figure. 6

- To draw a "**nmos**" select **p-well** from **LSW** window, select rectangle from layout window and draw a "**p-well**". Similarly, draw an n^+ region and then an active region without violating the DRC rules. Follow the same procedure to draw the layout of a "**pmos**". While drawing the layout make sure to save the design from time to time. Also verify for the correctness of the design by selecting **Verify→DRC** from the Layout window.
- Use metal1 to connect the active region to the sources (VDD and GND), the metal1 layer and the active region has to be connected through a contact. Metal2 can be connected to metal1 through via. Note that metal2 cannot be directly connected to the active region, it has to be connected to the metal1 layer first and then this metal1 can be connected to the active region.

- Poly has to be used for the gate.

Creating pins

Pins can be created by selecting **Create→Pin** from the layout window.

For example, to create a supply pin, select **Create→Pin** and type the Pin name as "**Vdd!**". Note that the pin name for the supply voltage has to start with uppercase v (V), which is shown in Fig.8. Select the IO type as "**Inputoutput"** and the pin has to be the same type as the layer on which it goes. In other words if the pin is to be placed on metal1, it has to be of type metal1. Use meaningful names for inputs and outputs, select the IO type as Input or Output depending on the desired pin type.

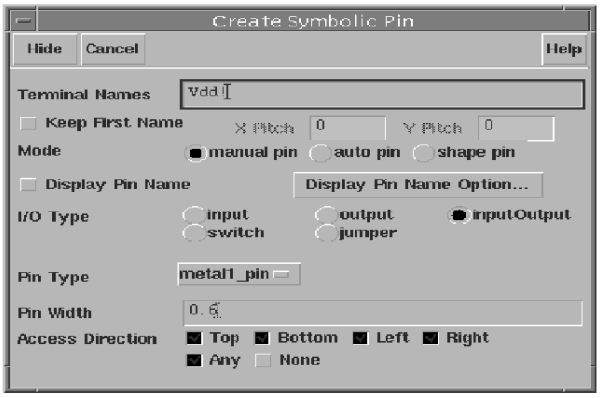

Figure. 7

Use labels to name the pins and the design. To print the label name select **Create→Pin** and type the label name as "**Vdd!**"

There are a few commands that can mapped to keys:

Command	**Key**
Stretch	s
Copy	c
Move	m
Delete	del
Rotate	O
Undo	u

(e) After the design is completed, it has to be saved by typing **Design→Save** from the layout window.

(f) The design so saved has to be verified by typing **Verify→DRC** from the layout window.

The number of errors and warnings, if any in the design would be shown in the icfb window. Also the errors and warnings would be shown with blinking signs in the layout window.

The reason for warning or error can be know by selecting **Verify→Markers→Explain** from the layout window and then clicking on the blinking part in the layout. The errors have to be corrected before going to the next step.
The extracted view has to be verified by selecting **Verify→Extract**

(g) A new window with the extracted design will open which will be much similar to the layout window.