EEL 5344C Digital CMOS VLSI Design Fall 2003 Handout on CADENCE Virtuoso Layout RA: Karthikeyan Lingasubramanian

Creating a library

- a. Start icfb by typing this command at grad Sun Server: icfb &
- b. Create a new library by selecting file → New → library from icfb window (Fig.1)



Fig.1

A window pops up (Fig. 2). Let the library name be "mylib".

				Ne	w Library			
0	ок	Cancel	Defaults	Apply		Help		
Library Technology File								
Na Di Mi ix ir ne	ame irector 1_M2 2_M3 n nvert stal1 home/	mylib y (non-li pin csec1/sau	brary direc mudral/my	tories)	If you will be creating mask layou other physical data in this library, will need a technology file. If you to use only schematic or HDL dat technology file is not required. Compile a new techfile Attach to an existing techfile Don't need a techfile	it or , you plan a, a		
Design Manager No DM =								

Fig.2

When you click "**ok**", a window pops up (Fig. 3) asking for ASCII technology file, enter the file name as "**project.tf**".

Load Technology File							
OK Cancel Defaults Ap			Apply	Help			
	chnology	File	project.tf				
Now Tec	choology l	ibrary	mylib				

Fig.3

c. Go to the terminal(Sun Server) and copy the following files "divaDRC.rul" and "divaEXT.rul" to "mylib" directory.

Sun Server: cp divaDRC.rul divaEXT.rul ./mylib

 Library Manage 	r: WorkArea: /home/cs	ee1/samudral	1					
<u>File Edit View D</u> esign Ma	nager	Help						
Show Categories Show Files								
Library	Cell	View						
Inylib	ľ	Ľ						
US 80ths shdllab analogib basic cdsDefFechlib functional Wylbb rfExemples rfLib sample	M1_M2 M2_M3 metall_pin metal2_pin metal3_pin poly_pin							
Messages								
Verning: The directory: '/home/cses1/samudral/lib' does not exist but was defined in libFile '/home/cses1/samudral/cds.lib' for Lib 'lib'.								

Fig.4

Creating a New Cell view

d. Create a cell view by selecting **File** \rightarrow **New** \rightarrow **Cellview** from icfb window (Fig.1).

Select the library name as "**mylib**"(the library name that you entered before) and type the cell name, say "**Inverter**" and select the Tool as "**Virtuoso**" as in Fig.5.

Create New File								
ок	Cancel	Defaults Help						
Library Name mylib								
Cell Name inverter]								
View Nan	ne 1	layout						
Tool		Virtuoso						
Library path file								
/home/cseel/samudral/cds.libj								

Fig.5 Click "**ok**" the LSW and layout window opens as in fig.6 and Fig.7.

- 	2.0	N 11	1	453	Virtus	oso* Lay	out Edi	ting: r	nylib inv	erter I	uvout.	_	_		
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- To draw a "**nmos**" select **p-well** from LSW window, select rectangle from layout window and draw a "**p-well**", make sure that the width is atleast 2µm as mentioned in the DRC rules sheet given to you. Draw n⁺ region and then an active region without violating the DRC rules. Follow the same procedure to draw the layout of a "**pmos**". While drawing the layout make sure to save the design from time to time. Also verify for the correctness of the design by selecting Verify→DRC from the Layout window.
- Use metall to connect the active region to the sources (VDD and GND), the metall layer and the active region has to be connected through a contact. Metal2 can be connected to metall through via. Note that metal2 cannot be directly connected to the active region, it has to be connected to the metall layer first and then this metall can be connected to the active region.





• Poly has to be used for the gate.

Creating pins

Pins can be created by selecting Create \rightarrow Pin from the layout window.

For example, to create a supply pin, select $Create \rightarrow Pin$ and type the Pin name as "Vdd!". Note that the pin name for the supply voltage has to start with uppercase v (V), which is shown in Fig.8. Select the IO type as "Inputoutput" and the pin has to be the same type as the layer on which it goes. In other words if the pin is to be placed on metall, it has to be of type metall. Use meaningful names for inputs and outputs, select the IO type as Input or Output depending on the desired pin type.

-	Create S	Symbolic Pin	
Hide Cancel			Help
Terminal Names	Vdd ∏		
🔲 Keep First Nam	e X Pitch	0 Y (stch 0
Mode	💼 manual pir	i 🔵 auto pin 🤇)shape pin
📃 Display Pin Na	ne	Display Pin Na	me Option
І/О Туре	Switch	Output jumper	🛑 inputOutput
Pin Type	metal1_pin =		
Pin Width	0.6		
Access Direction	M Top M Be M Any No	ottom 🖬 Left one	Right

Fig.8

Use labels to name the pins and the design. To print the label name select **Create** \rightarrow **Pin** and type the label name as "Vdd!"

There are a few commands that can mapped to keys:

Command	Key
Stretch	S
Сору	с
Move	m
Delete	del
Rotate	0
Undo	u

- e. After the design is completed, it has to be saved by typing **Design→Save** from the layout window.
- **f.** The design so saved has to be verified by typing Verify \rightarrow DRC from the layout window.

The number of errors and warnings, if any in the design would be shown in the icfb window. Also the errors and warnings would be shown with blinking signs in the layout window.

The reason for warning or error can be know by selecting **Verify** \rightarrow **markers** \rightarrow **Explain** from the layout window and then clicking on the blinking part in the layout. The errors have to be corrected before going to the next step.

The extracted view has to be verified by selecting Verify → Extract

g. A new window with the extracted design will open which will be much similar to the layout window.