EEL 5344C Digital CMOS VLSI Design
Fall 2003
Handout on CADENCE Virtuoso Layout

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Creating a library

a. Start `icfb` by typing this command at grad
`Sun Server:` **`icfb &`**

b. Create a new library by selecting **file → New → library** from icfb window (Fig.1)

Fig.1

A window pops up (Fig. 2). Let the library name be "**mylib**".

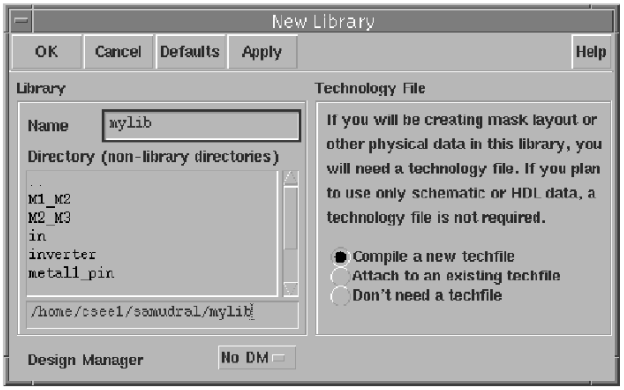

Fig.2

When you click "**ok**", a window pops up (Fig. 3) asking for ASCII technology file, enter the file name as "**project.tf**".

Fig.3

c. Go to the terminal(Sun Server) and copy the following files "**divaDRC.rul**" and "**divaEXT.rul**" to "**mylib**" directory.
Sun Server**: cp divaDRC.rul divaEXT.rul ./mylib**

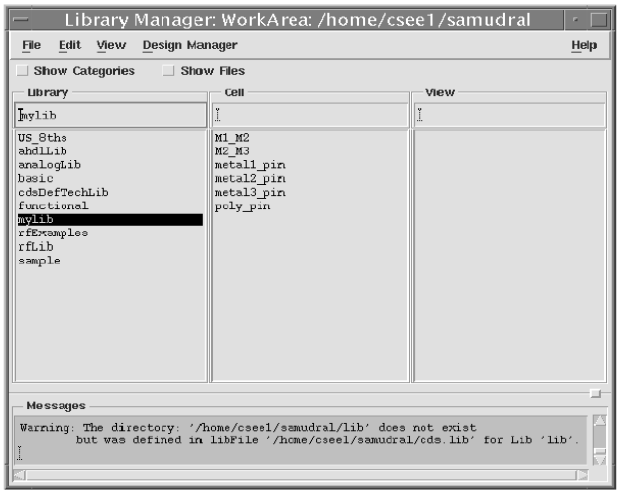

Fig.4

Creating a New Cell view

d. Create a cell view by selecting **File→New→Cellview** from icfb window (Fig.1).

Select the library name as "**mylib**"(the library name that you entered before) and type the cell name, say "**Inverter**" and select the Tool as "**Virtuoso**" as in Fig.5.

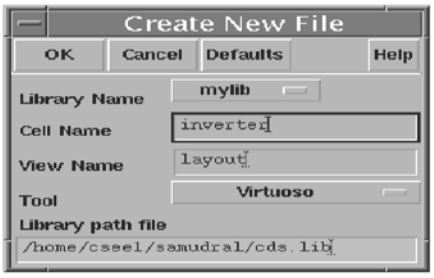

Fig.5

Click "**ok**" the LSW and layout window opens as in fig.6 and Fig.7.

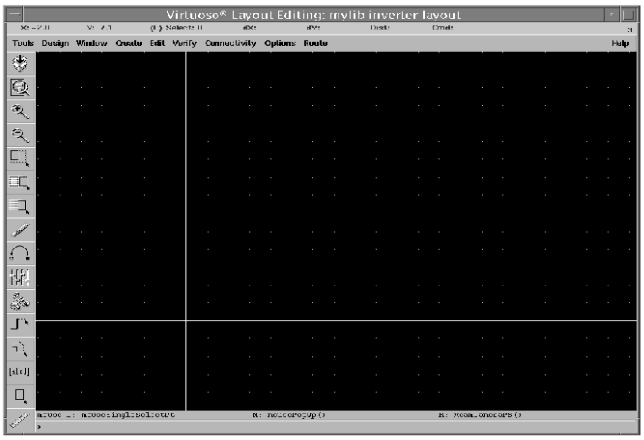

Fig.6

- To draw a "**nmos**" select **p-well** from LSW window, select rectangle from layout window and draw a "**p-well**", make sure that the width is atleast 2µm as mentioned in the DRC rules sheet given to you. Draw n^+ region and then an active region without violating the DRC rules. Follow the same procedure to draw the layout of a "**pmos**". While drawing the layout make sure to save the design from time to time. Also verify for the correctness of the design by selecting **Verify→DRC** from the Layout window.
- Use metal1 to connect the active region to the sources (VDD and GND), the metal1 layer and the active region has to be connected through a contact. Metal2 can be connected to metal1 through via. Note that metal2 cannot be directly connected to the active region, it has to be connected to the metal1 layer first and then this metal1 can be connected to the active region.

Fig.7

- Poly has to be used for the gate.

Creating pins

Pins can be created by selecting **Create→Pin** from the layout window.

For example, to create a supply pin, select **Create→Pin** and type the Pin name as "**Vdd!**". Note that the pin name for the supply voltage has to start with uppercase v (V), which is shown in Fig.8. Select the IO type as "**Inputoutput"** and the pin has to be the same type as the layer on which it goes. In other words if the pin is to be placed on metal1, it has to be of type metal1. Use meaningful names for inputs and outputs, select the IO type as Input or Output depending on the desired pin type.

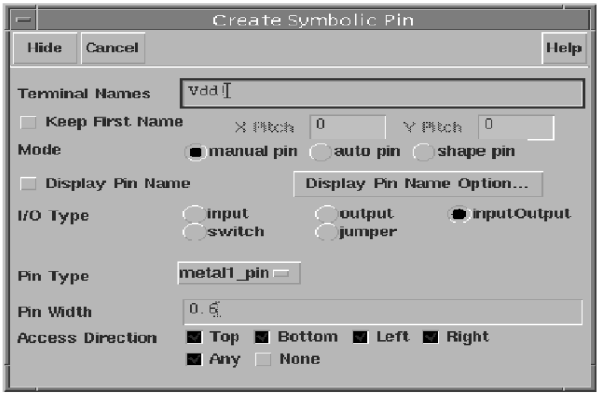

Fig.8

Use labels to name the pins and the design. To print the label name select **Create→Pin** and type the label name as "**Vdd!**"

There are a few commands that can mapped to keys:

Command	**Key**
Stretch	s
Copy	c
Move	m
Delete	del
Rotate	O
Undo	u

e. After the design is completed, it has to be saved by typing **Design→Save** from the layout window.

f. The design so saved has to be verified by typing **Verify→DRC** from the layout window.

The number of errors and warnings, if any in the design would be shown in the icfb window. Also the errors and warnings would be shown with blinking signs in the layout window.

The reason for warning or error can be know by selecting **Verify→markers→Explain** from the layout window and then clicking on the blinking part in the layout. The errors have to be corrected before going to the next step.
The extracted view has to be verified by selecting **Verify→Extract**

g. A new window with the extracted design will open which will be much similar to the layout window.